

WHAT IS CLAIMED IS:

1 (1) In a digital intermediate frequency downconversion circuit for
2 downconverting in-phase and quadrature signal components of a digitized communication
3 signal, a method for processing the in-phase and quadrature signal components of the digital
4 signal comprising:
5 processing a single serial digital bit stream formed of the in-phase and
6 quadrature signal components through a set of simple logic to produce a digital representation
7 of downconverted in-phase and quadrature components; and
8 recombining the digital representation of the downconverted in-phase and
9 quadrature components with a reconstruction filter in a manner to obtain a digital
10 representation of a baseband signal substantially free of image artifacts.

1 2. The method according to claim 1 further including the steps of:
2 employing an oversampled digital word of four bits in length from a source
3 digital oscillator as a reference signal;
4 supplying digital signal mixers with said reference signal to achieve at least
5 sixteen levels of accuracy as a sine wave mixing signal without significant phase or
6 amplitude error;
7 mixing the digitized serial bit stream according to a clock with output of a
8 four-bit wide table representing the reference signal;
9 recombining digitally the in-phase and quadrature signals to obtain a digitally
10 combined signal; and
11 binary weighting the combined signal into a digital reconstruction filter to
12 produce a downconverted signal is unaffected by resistor tolerance.

1 (3) In a digital IF downconversion circuit for downconverting in-phase
2 and quadrature signal components of a digitized communication signal, a processor for in-
3 phase and quadrature signal components of the digital signal comprising:
4 logic for processing a single serial digital bit stream formed of the in-phase
5 and quadrature signal components to produce a digital representation of downconverted in-
6 phase and quadrature components; and
7 a digital reconstruction filter for recombining the digital representation of the
8 downconverted in-phase and quadrature components in a manner to obtain a digital
9 representation of a baseband signal substantially free of image artifacts.

1 4. The circuit according to claim 3 further including:
2 a source digital oscillator supplying digital signal mixers with an oversampled
3 digital word of four bits in length to achieve at least sixteen levels of accuracy for a sine wave
4 mixing signal without significant phase or amplitude error.

1 5. The circuit according to claim 1 further including resistor means
2 coupled to input of the digital reconstruction filter for binary weighting the digital
3 recombined signal produce a downconverted signal is unaffected by resistor tolerance.

1 6. A method of image rejection processing of a received RF signal,
2 comprising:
3 performing downconversion of the received RF signal to produce analog I and
4 Q signals; and
5 for each of the analog I signal and the analog Q signal:
6 oversampling the analog signal to obtain an oversampled digital signal;
7 producing a periodic oversampled digital reference signal; and
8 logically combining the digital signal with the digital reference signal
9 to produce an image-canceled digital baseband signal.

1 7. The method of claim 6, comprising:
2 converting the digital baseband signal to an analog baseband signal.

1 8. An image reject circuit apparatus comprising:
2 — a first frequency downconversion circuit employing a first local oscillator for
3 downconverting in-phase and quadrature signal components of a digitized communication
4 signal to a first intermediate frequency;
5 — sigma delta converters for generating an in phase digital bit stream and a
6 quadrature phase digital bit stream;
7 — a digital in-phase and quadrature phase second local oscillator;
8 mixing circuitry for mixing respective single serial digital bit stream in-phase
9 signal and single serial digital bit stream quadrature phase signal through a set of logic gates
10 to produce a digital representation of downconverted in-phase and quadrature components;
11 and

weighting resistances in series with the outputs of the logic gates for combining the digital representation of the downconverted in-phase and quadrature components according to value in an in-phase signal and in a quadrature phase signal; and reconstruction filters to recover in-phase and quadrature phase baseband signals from said downconverted in-phase and quadrature components substantially free of image artifacts.

9. The image reject circuit apparatus according to claim 8 wherein said mixing circuitry comprises, for each significant bit:

first and second exclusive-OR gates coupled to receive as first input an in phase digital bit stream and as second inputs a high accuracy sine function bit stream and a high accuracy cosine function bit stream;

third and fourth exclusive-OR gates coupled to receive as first input a quadrature phase digital bit stream and as second inputs a high accuracy sine function bit stream;

first OR gate for logically adding the outputs of the first and second XOR gates for the in-phase channel;

first AND gate for logically multiplying the outputs of the first and second XOR gates for the in-phase channel;

second OR gate for logically adding the outputs of the third and fourth XOR gates for the quadrature phase channel; and

second AND gate for logically multiplying the outputs of the third and fourth XOR gates for the quadrature phase channel.

10. The circuit apparatus according to claim 9 wherein the reconstruction filter comprises:

weighting resistors for each output of each of the first and second AND gates and first and second OR gates, said weighting resistors defining a binary weight for its corresponding bit;

a first lowpass filter means at a first combining node of the first AND gate and first OR gate;

a second lowpass filter means at a second combining node of the second AND gate and second OR gate;

